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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Martin M. Deneroff, et al.
Serial No.:	09/315,806
Filing Date:	May 21, 1999
Group Art Unit:	2181
Examiner:	Paul R. Myers
Title:	SYSTEM AND METHOD FOR PROVIDING ACCESS TO A BUS

BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

APPEAL BRIEF

Applicant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner mailed May 8, 2002 finally rejecting Claims 1-20. Applicant filed a Notice of Appeal on August 7, 2002. Applicant respectfully submits herewith their brief on appeal, in triplicate, with a statutory fee of $320.00.

REAL PARTY IN INTEREST

The present application was assigned to Silicon Graphics, Incorporated, a Delaware corporation, as indicated by an assignment from the inventors recorded on May 21, 1999 in the Assignment Records of the United States Patent and Trademark Office at Reel 9983, Frames 0920-0923.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-20 stand rejected pursuant to a Final Action mailed May 8, 2002. Claims 1-20 are all presented for appeal.

STATUS OF AMENDMENTS

A Response to Examiner's Final Action was filed on July 8, 2002 in response to the Final Action mailed May 8, 2002. No amendments were made to the claims. The Examiner issued an Advisory Action dated July 23, 2002 which stated that the Response to Examiner's Final Action was considered but was not persuasive to overcome the rejection of the claims. A Notice of Appeal was filed on August 7, 2002.

SUMMARY OF INVENTION

A computer system (10) includes a bus controller (12), a bus (14), a plurality of processing devices (16), and a plurality of enabling switches (18). Each enabling switch (18) corresponds to a separate one of the processing devices (16). Each processing device (16) sends an access request (24) to arbitration logic (22) in the bus controller (12) requesting access to the bus (14). The arbitration logic (22) selects one of the access requests (24) according to a priority protocol. The arbitration logic (22) generates a control signal (20) associated with the selected access request (24). The control signal (20) is provided to the enabling switch (18) corresponding to the processing device (16) that sent the selected access request(24). The enabling switch (18) enables access to the bus (14) for the processing device (16) in response to the control signal (20). In this manner, the computer system (10) can limit a number of processing devices (16) having access to the bus (14) in order to control a load on the bus (14).

STATEMENT OF ISSUES

1. Did the Examiner err in concluding that Claims 1-20 were obvious under 35 U.S.C. §103(a) over U.S. Patent No. 5,396,602 Amini, et al in view of U.S. Patent No. 3,470,542 Trantanella?

GROUPING OF CLAIMS

Applicant respectfully requests that Claims 1-20 be grouped to stand or fall together according to 37 C.F.R. § 1.192(c)(7).

ARGUMENT

1. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Amini, et al in view of Trantanella. According to M.P.E.P. §2143, to establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation to combine the references. Second, there must be a reasonable expectation of success. Third, the prior art combination of references must teach or suggest all the claim limitations. The Examiner has not established that any criteria for a prima facie case of obviousness has been met in this instance.

First, there is no suggestion or motivation in the Amini, et al. and Trantanella patents to combine them as proposed by the Examiner. The Amini, et al. patent is directed to an arbitration mechanism for a multiple bus computer system that includes several devices attached to a PCI bus that generate bus access requests for and receive bus access grants from a system arbitration control point. The Trantanella patent is directed to a modular system design where all of the interface units are tied to the common bus lines so that all devices associated with the interface units can freely communicate with each other without using request and grant signaling means for bus access. Thus, none of the cited patents are related to any common subject matter. The Examiner has not cited any language within either of the Amini, et al. or Trantanella patents that would suggest any capability for them to be combined. In fact, no reason was provided by the Examiner for combining the references as has been proposed. The Examiner has merely provided conclusory "it would have been obvious to combine" statements using improper hindsight reconstruction without any support for such conclusory statements from any of the cited patents. A statement that modifications of the prior art to meet the claimed invention

would have been well within the ordinary skill of the art at the time the claimed invention was made because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references. See M.P.E.P. 2143.01. Since the Examiner has not provided any reasoning, let alone objective reasoning, the burden to establish the first criteria of a prima facie case of obviousness has not been met.

Moreover, the proposed modification changes the principle of operation of the prior art being modified. The Amini, et al. patent specifically requires a request and grant signaling technique for a particular device on a PCI bus to communicate over the PCI bus despite having other devices connected to the PCI bus while the Trantanella patent merely discloses assigning input, output, and control roles to all of the interface units on its common bus with the ability to add other interface units at any point on the common bus and allow every device to freely communicate with every other device on the common bus. Thus, the principle of operation of the Amini, et al. patent to obtain bus access prior to providing communications would be improperly changed by incorporating Trantanella's ability to freely communicate over a common bus. The Examiner has yet to explain how the Trantanella patent can be combined with the Amini, et al. patent in view of such different functionalities. Therefore, Applicant respectfully submits that the Examiner has failed to establish the first criteria for a prima facie case of obviousness.

Second, a reasonable expectation of success has not been shown by the Examiner. The combination of the Amini, et al. and Trantanella patents would not be capable of performing the operation required by the claimed invention. There is no

showing by the Examiner that the ability to communicate freely over a common bus as disclosed in the Trantanella patent would be able to operate in the request/grant implementation of the Amini, et al. patent. There has also been no showing that the combined references would even be able to perform the ability to control what devices can be connected to a bus as required by the claimed invention. The proposed combination attempts to combine incompatible processing techniques that have not been shown to be capable of operating according to any degree of predictability. The Examiner, without the improper hindsight look through the claimed invention, has not addressed that the proposed combination of the Amini, et al. and Trantanella patents would have any success whatsoever let alone a reasonable expectation of success. Therefore, Applicant respectfully submits that the Examiner has failed to establish the second criteria for a prima facie case of obviousness.

Third, the Examiner has not shown that the proposed Amini, et al. - Trantanella combination teaches or suggests all of the claim limitations. For example, Independent Claims 1, 11, and 17 provide for enabling a switch or pass transistor to control connection and access of a device to a bus. By contrast, the Amini, et al. patent and the Trantanella patent both provide continuous access and connection of their respective devices and interface units to a common bus. Neither the Amini, et al. patent nor the Trantanella patent disclose an ability to limit access to a bus let alone through the use of a switch or pass transistor as required by the claimed invention. In fact, the Examiner readily admits that the Amini, et al. patent has no such element to control access to a bus. The Examiner attempts to use the Trantanella patent to support the limitation of a switch or pass transistor

however the Trantanella patent clearly shows in its FIGURE 3 that the in-out buffers are always connected to the bus lines.

Moreover, the Examiner has not shown how the proposed combination teaches each and every limitation of the dependent claims. For example, dependent Claims 3, 16, and 20 require a PCI bus operating at a frequency of at least 66 MHz. The Examiner took official notice that 66 MHz and 100 MHz PCI busses were common in the art but failed to address how the system of the Amini, et al. patent addresses the loading problem at such frequencies or how the system of the Amini, et al. patent could operate at such a frequency with all of the peripheral devices connected to its PCI bus and overloading the PCI bus. Applicant respectfully requests the Examiner to provide a reference to support the well known in the art basis for rejection these claims. Dependent Claim 6 allows access to the bus for a particular device prior to an end of access to the bus by another device. Neither the Amini, et al. patent nor the Trantanella patent disclose such a capability. Dependent Claims 9 and 12 provide for controlling a load on the bus. By contrast, the Amini, et al. and Trantanella patents have no concern for the load on a bus as all of their respective devices and interface units are always connected to the respective bus. The Examiner merely states that the limitations of each and every claim are found in the cited references but still fails to specifically cite where within the cited references each limitation is disclosed. Therefore, Applicant respectfully submits that with respect to Claims 1-20 the Examiner has failed to establish the third criteria for a prima facie case of obviousness.

Applicant respectfully requests the Examiner to provide one or more combinable references that support the rejections of the claims. Applicant also respectfully requests the Examiner to show where each and every limitation of each and

every claim is taught or suggested by the prior art. With no other supporting reference that is combinable with the Amini, et al. or Trantanella patents, all claim limitations have not been taught or suggested by the Examiner's currently proposed combination. The Examiner has not cited any language within the Amini, et al. or Trantanella patents, either alone or in combination, that would suggest the desirability of making the claimed invention or providing any motivation to do so. Subjective conclusions of obviousness are not sufficient to establish a prima facie case of obviousness without some objective reason to modify and combine the prior art references. Therefore, Applicants respectfully submit that Claims 1-20 are patentably distinct from the proposed Amini, et al. - Trantanella combination.

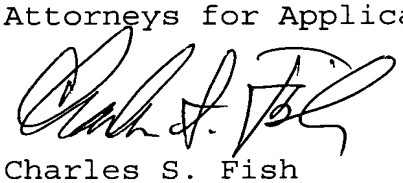
CONCLUSION

Applicant has clearly demonstrated that the present invention as claimed is clearly distinguishable over all the art cited of record, either alone or in combination, and satisfies all requirements under 35 U.S.C. §§101, 102, and 103, and 112. Therefore, Applicant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

Attached herewith is a check made payable to the "Commissioner of Patents and Trademarks" in an amount of $320.00 to satisfy the appeal brief filing fee of 37 C.F.R. §1.17(c).

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicant



Charles S. Fish
Reg. No. 35,870

2001 Ross Avenue, Suite 600
Dallas, TX 75201-2980
(214) 953-6507
October 7, 2002

APPENDIX A

1. (Previously Amended) A method of providing access to a bus, comprising:

receiving a request for access to the bus;

selecting the request according to a priority associated with the request;

generating a control signal in response to selection of the request;

enabling a switch associated with the request to provide access to the bus in response to the control signal.

2. The method of Claim 1, wherein the bus is a PCI bus.

3. The method of Claim 2, wherein the PCI bus operates at a frequency of at least 66 MHz.

4. The method of Claim 1, wherein the request is received from a device desiring to communicate over the bus.

5. (Previously Amended) The method of Claim 1, further comprising:

receiving a plurality of access requests for the bus, each of the plurality of access requests being received from one of a plurality of devices coupled to the bus, each of the plurality of devices having a switch associated therewith;

selecting a particular one of the plurality of access requests according to a predetermined priority protocol;

generating a control signal corresponding to the selected particular one of the plurality of access requests;

providing the control signal to a particular one of the plurality of devices that sent the selected particular one of the plurality of access requests, the control signal enabling the switch associated with the particular one of the plurality of devices to provide access to the bus.

6. (Previously Amended) The method of Claim 5, further comprising:

selecting a next one of the plurality of access requests according to the predetermined priority protocol;

generating a control signal corresponding to the selected next one of the plurality of access requests;

providing the control signal to a next one of the plurality of devices that sent the selected next one of the plurality of access requests, the control signal enabling the switch associated with the next one of the plurality of devices to provide access to the bus prior to an end of access to the bus for the particular one of the plurality of devices.

7. The method of Claim 6, further comprising:

determining an end of access to the bus for the particular one of the plurality of devices;

initiating access to the bus by the next one of the plurality of devices in response to the end of access to the bus for the particular one of the plurality of devices.

8. The method of Claim 7, further comprising:

generating a disabling control signal in response to the end of access to the bus for the particular one of the plurality of devices;

preventing the particular one of the plurality of devices from accessing the bus in response to the disabling control signal.

9. The method of Claim 1, further comprising:

limiting a number of generated control signals in order to control a load on the bus.

10. The method of Claim 1, further comprising:

generating a disable control signal for a request not selected in order to disable access to the bus.

11. (Previously Amended) A system for providing access to a bus, comprising:

a bus controller;

a plurality of processing devices coupled to the bus controller by a bus;

a plurality of enabling switches on the bus, each enabling switch coupled to a corresponding processing device, each enabling switch providing the corresponding processing device with access to the bus in response to a control signal from the bus controller.

12. The system of Claim 11, wherein the bus controller allows simultaneous access to the bus by a predetermined number of the plurality of processing devices in order to limit a load on the bus.

13. The system of Claim 11, wherein the bus controller receives a plurality of access requests from the plurality of processing devices for access to the bus.

14. The system of Claim 13, Wherein the bus controller arbitrates the plurality of access requests from the plurality of processing devices according to a predetermined protocol.

15. The system of Claim 11, wherein the bus is a PCI bus.

16. The system of Claim 15, wherein the PCI bus operates at a frequency of approximately 66 MHz.

17. (Previously Amended) A PCI bus, comprising:

a plurality of pass transistors, each pass transistor operable to provide an associated processing device with bus access, each pass transistor operable to receive a control signal to enable and disable bus access for its associated processing device.

18. The PCI bus of Claim 17, wherein a particular pass transistor receives an enable control signal in response to an access request sent by its associated processing device.

19. The PCI bus of Claim 17, wherein a particular pass transistor is operable to disable bus access for its associated processing device such that the particular processing device does not appear to be coupled to the PCI bus.

20. The PCI bus of Claim 17, wherein each of the processing devices is operable to communicate at a 66 MHz rate.